Amendments to the Specification

Please replace the current abstract with the following abstract beginning at page 26, line 1:

-- ABSTRACT

The present invention relates to a delay line for delaying an input signal. The input signal comprises a series of samples. The delay line is characterized in that it is configured to delay the input signal by a series of delays and that the delay line is divided into a series of delay sub-lines each being used to write one sample from the series of samples of the input signal, and in that it comprises control means configured to generate read addresses of the samples in the delay sub-lines from the series of samples of the input signal. The read addresses are equal to a difference between a write address of a sample in the delay sub-lines of the input signal and the delays expressed in a number of chip periods.--